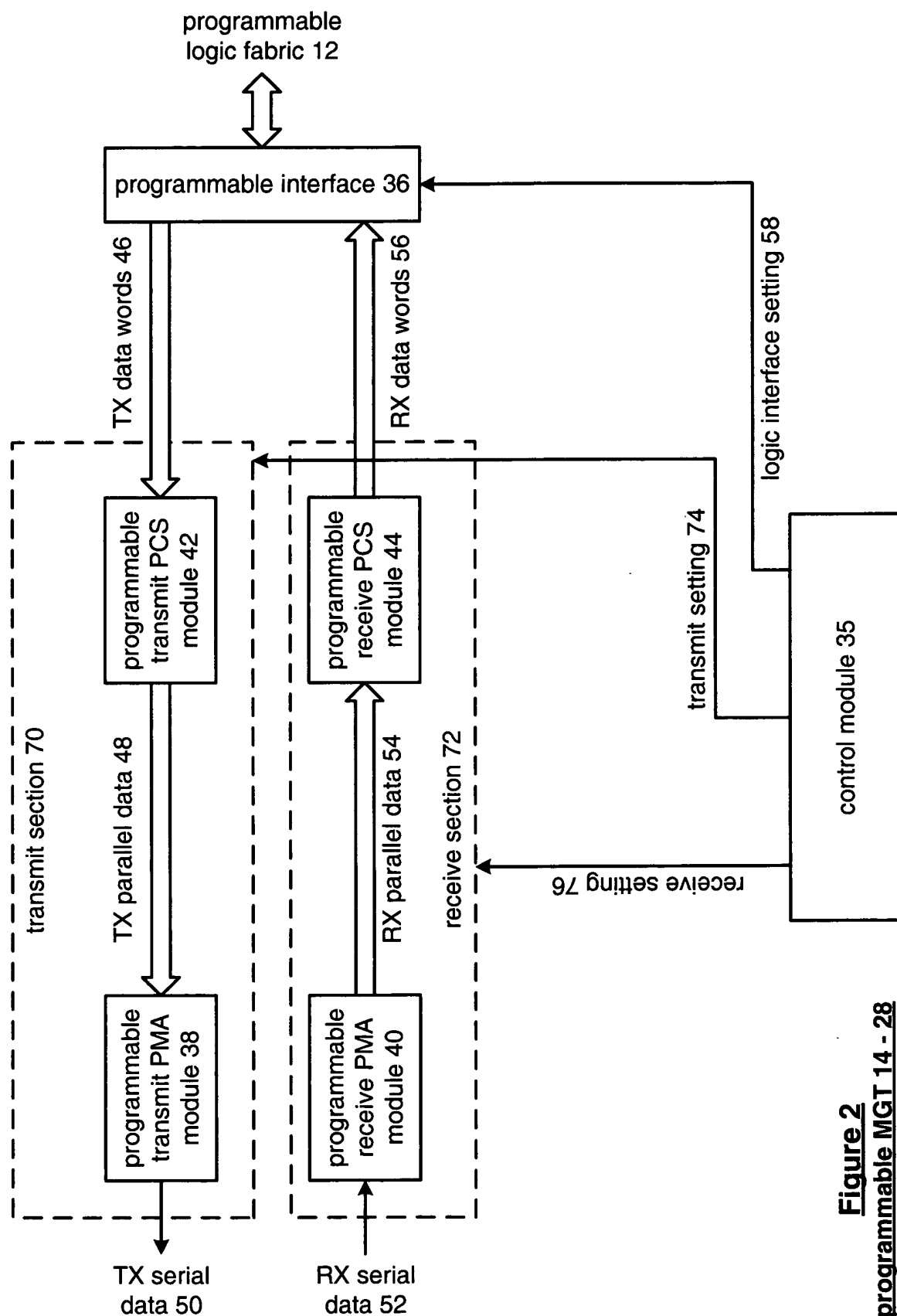
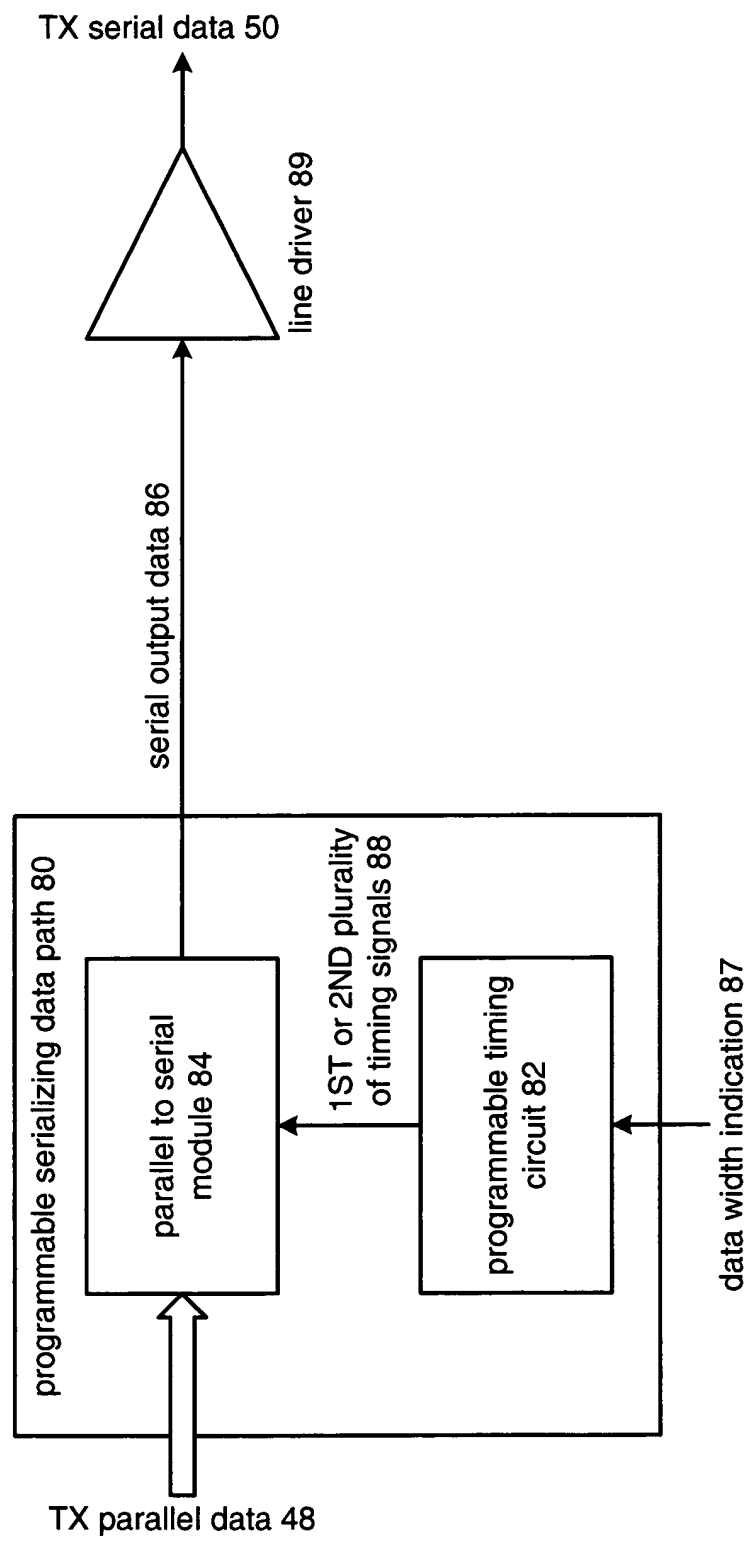


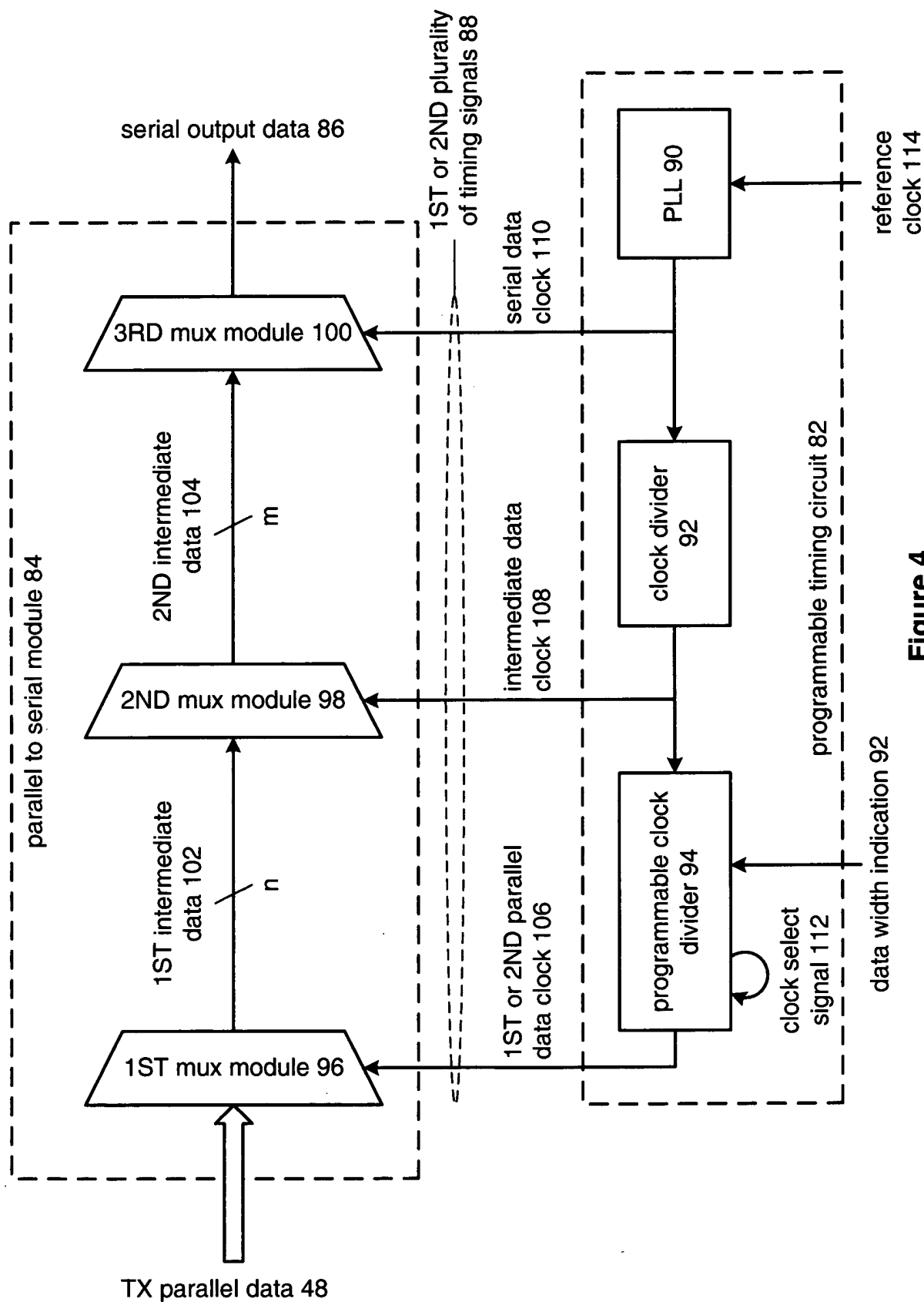
**Figure 1**  
**programmable**  
**logic device 10**



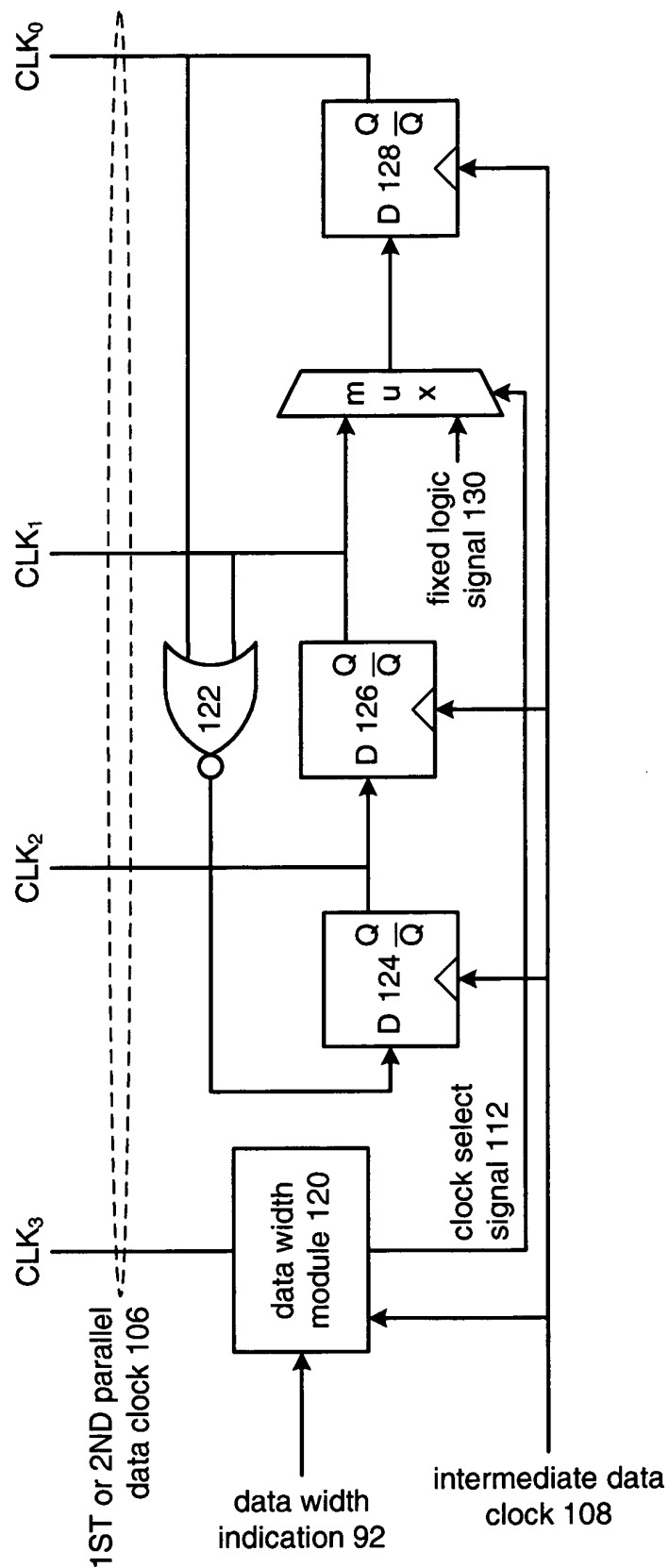
**Figure 2**  
**programmable MGT 14 - 28**



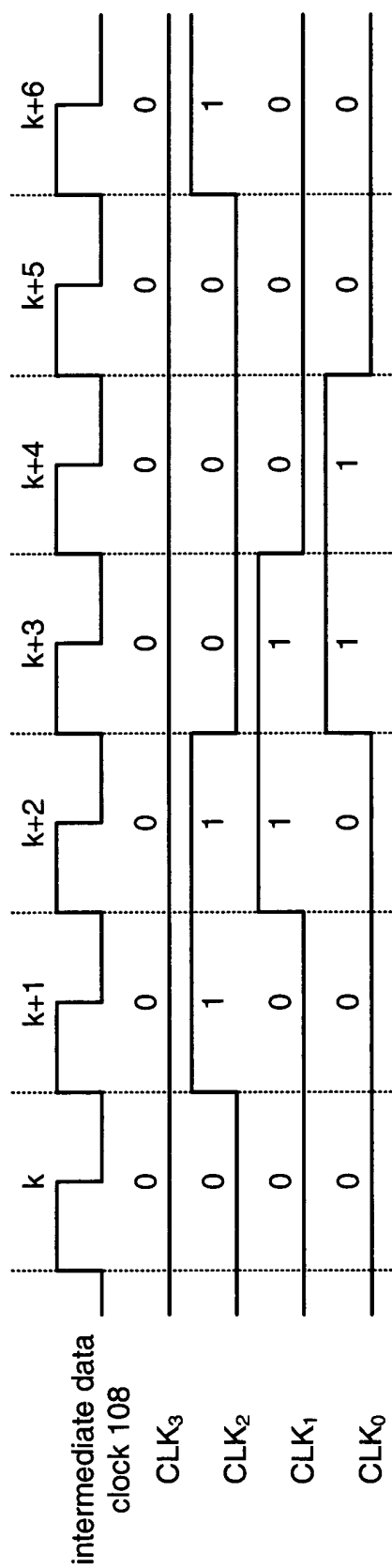
**Figure 3**  
programmable transmit  
PMA module 38



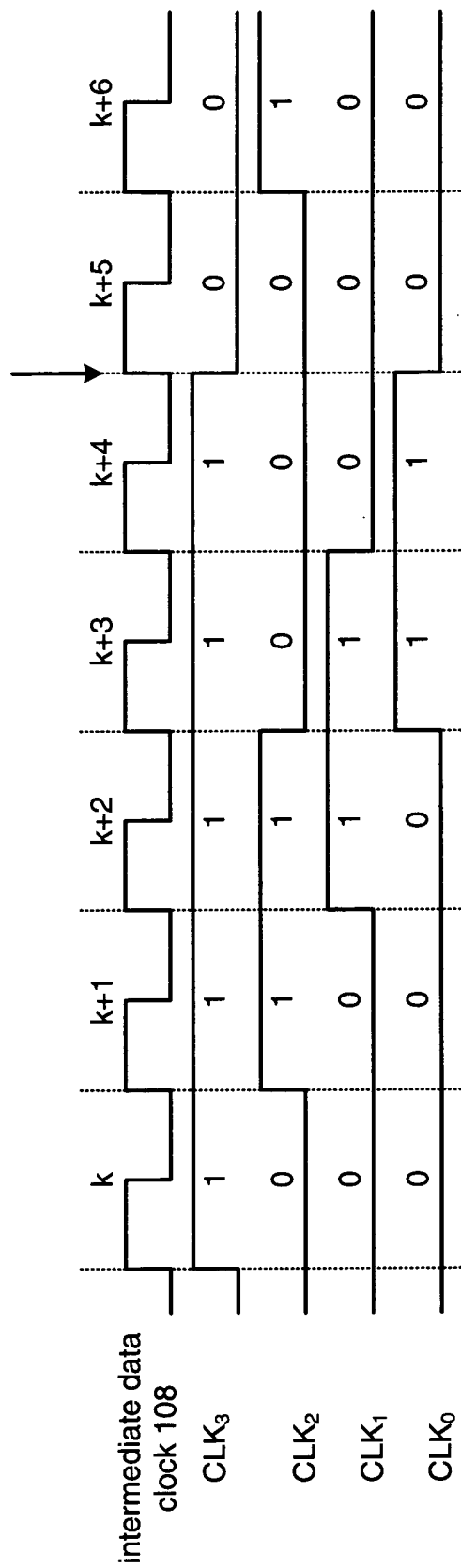
**Figure 4**  
programmable serializing data path 80



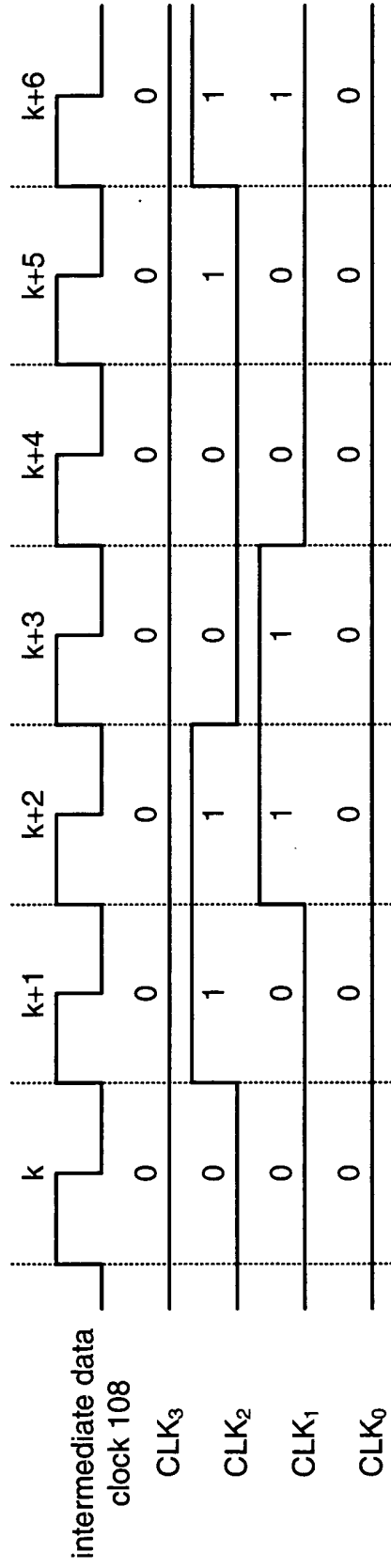
**Figure 5**  
**programmable clock divider 94**



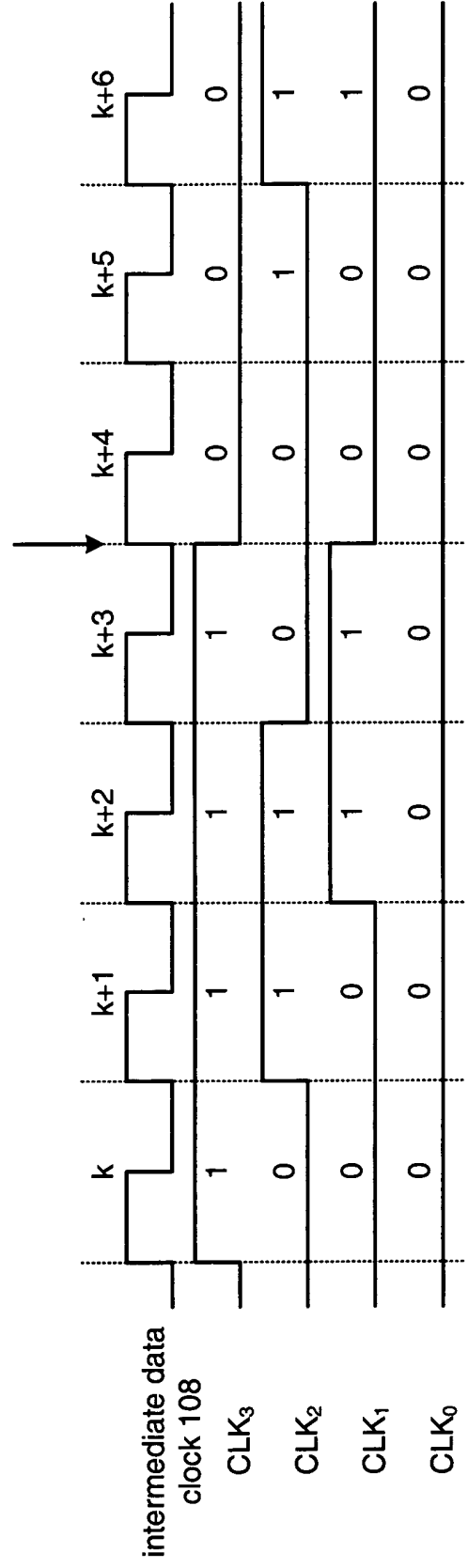
**Figure 6**  
timing diagram of programmable clock divider  
94 for 20 bit parallel input data



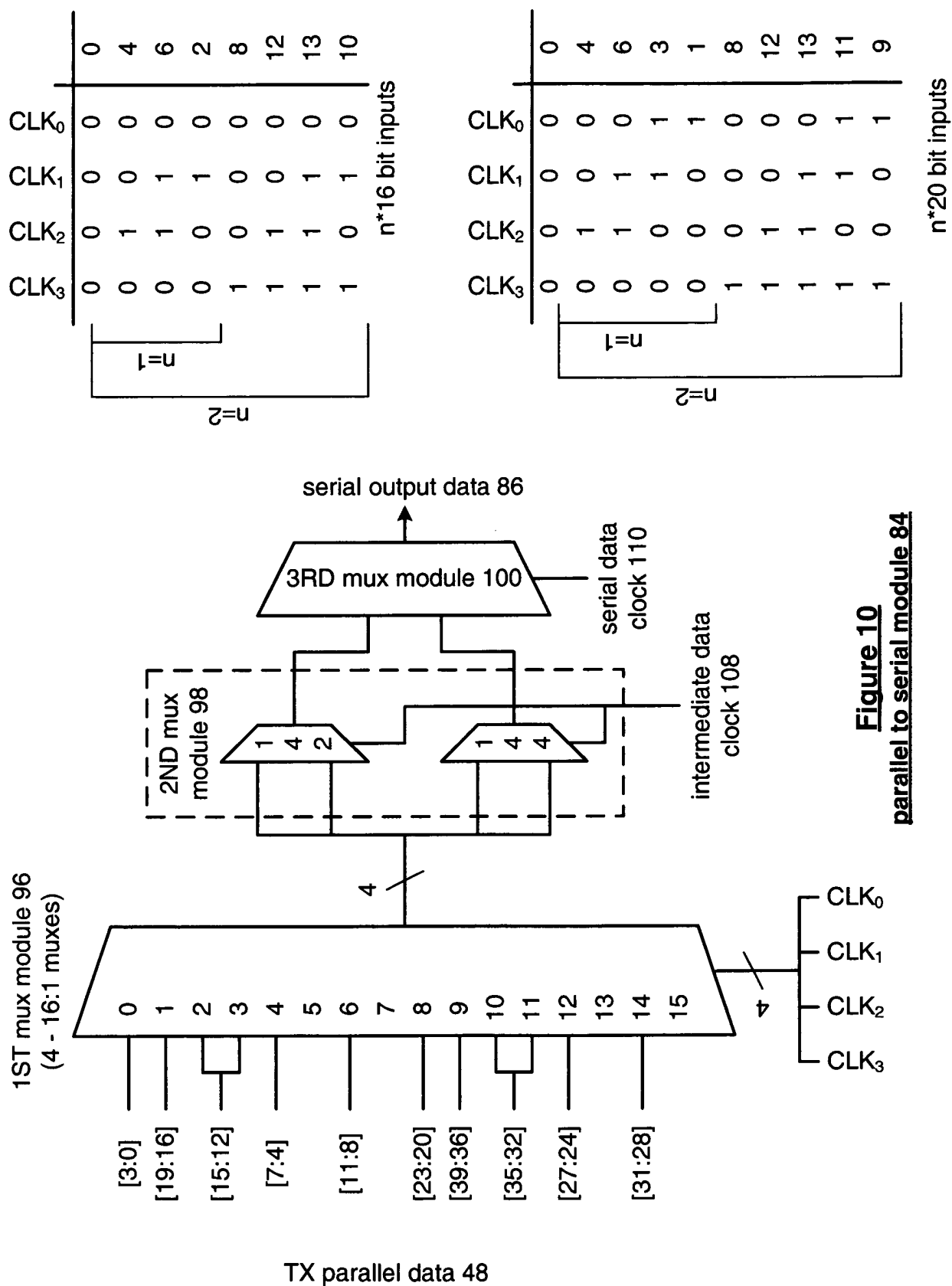
**Figure 7**  
timing diagram of programmable clock divider  
94 for 40 bit parallel input data



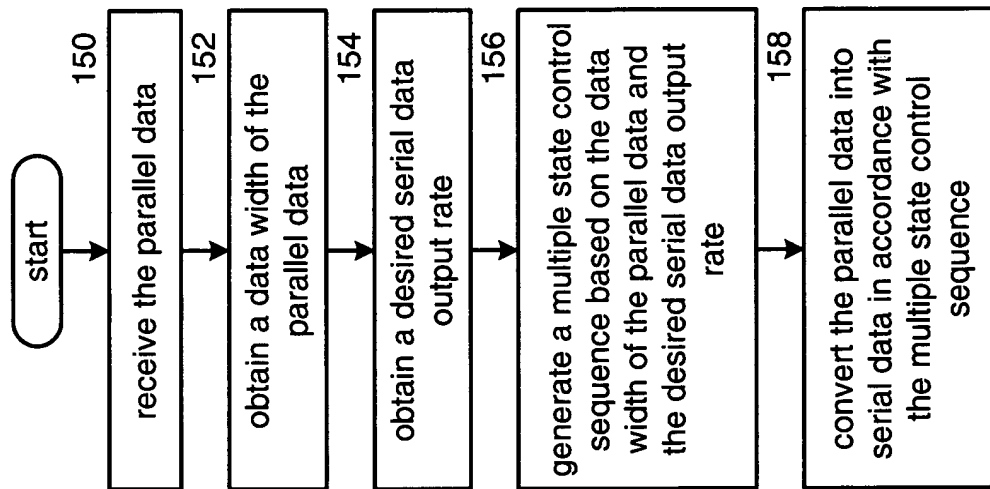
**Figure 8**  
timing diagram of programmable clock divider  
94 for 16 bit parallel input data



**Figure 9**  
timing diagram of programmable clock divider  
94 for 32 bit parallel input data







**Figure 11**